

What is claimed is:

1 1. A semiconductor protection element comprising:
2 a semiconductor substrate having a first region of a first
3 impurity concentration and a pair of second regions having a
4 second impurity concentration being higher than that of said first
5 region; and
6 silicide layers each being formed in a manner so as to be
7 in contact with a surface of each of said second regions;
8 wherein said first region has a first surface region not
9 covered with said silicide layers and said second regions have
10 second surface regions not covered with said silicide layers and
11 said first surface region is sandwiched by two said second surface
12 regions;
13 wherein each of said silicide layers is formed in a manner
14 that each of said second surface regions is in contact with said
15 first surface region in a continued manner and that each of said
16 second surface regions is exposed; and
17 wherein each of said silicide layers makes up a low
18 resistance region having a relatively low resistance value, each
19 of said second surface regions makes up an intermediate resistance
20 region having an intermediate resistance value, and said first
21 surface region makes up a high resistance region having a
22 relatively high resistance value.

1 2. The semiconductor protection element according to Claim 1,
2 wherein a field oxide film is formed on said first surface region
3 or on said first exposed region.

1 3. The semiconductor protection element according to Claim 1,
2 wherein a gate electrode structure is formed on said first surface
3 region or on said first exposed region.

1 4. A semiconductor protection element comprising:
2 a semiconductor substrate having a first region of a first
3 impurity concentration and a pair of second regions having a
4 second impurity concentration being higher than that of said first
5 region; and
6 silicide layers each being partially formed in a manner so
7 as to be in contact with a surface of said second regions;
8 wherein said first region has a first exposed region being
9 exposed on a surface of said semiconductor substrate and each of
10 said silicide layers is so formed as to have a second exposed region
11 in which part of each of said second regions is exposed on a surface
12 of said semiconductor substrate in a manner so as to continuously
13 be in contact with said first exposed region;
14 wherein said first exposed region is sandwiched by two said
15 second regions; and
16 wherein each of said silicide layers makes up a low
17 resistance region having a relatively low resistance value, each
18 of said second exposed regions in said second region makes up an
19 intermediate resistance region having an intermediate resistance
20 value, and said first exposed region in said first region makes
21 up a high resistance region having a relatively high resistance
22 value.

1 5. The semiconductor protection element according to Claim 4,
2 wherein said first region is made up of a well region.

1 6. The semiconductor protection element according to Claim 4,
2 wherein said first region is formed on a surface of said
3 semiconductor substrate and in a manner that said first region
4 and said second region are overlapped on a surface of said
5 semiconductor substrate.

1 7. The semiconductor protection element according to Claim 6,
2 wherein, said first impurity concentration of said first region,
3 when it is assumed that a well region is formed on said
4 semiconductor substrate, is higher than that of said well region.

1 8. The semiconductor protection element according to Claim 4,
2 wherein a field oxide film is formed on said first surface region
3 or on said first exposed region.

1 9. The semiconductor protection element according to Claim 4,
2 wherein a gate electrode structure is formed on said first surface
3 region or on said first exposed region.

1 10. The semiconductor protection element according to Claim 4,
2 wherein said second exposed region has a surface length being
3 equal to or larger than that of said first exposed region.

1 11. The semiconductor protection element according to Claim 4,
2 wherein a surface length of said second exposed region is equal
3 to or larger than a depth of said second region.

1 12. A semiconductor protection element comprising:

2 a semiconductor substrate having a first region of a first
3 impurity concentration and a pair of second regions having a
4 second impurity concentration being higher than that of said first
5 region;

6 wherein said first region is made up of a well region;

7 wherein, on said first region, a third region of a third
8 impurity concentration being higher than said first impurity
9 concentration and being lower than said second impurity
10 concentration is formed;

11 wherein said third region is sandwiched by two said second
12 regions, makes up a first exposed region being exposed on a surface
13 of said semiconductor substrate and, on a surface of said
14 semiconductor substrate, said third region and said second region
15 are overlapped each other;

16 wherein each of said silicide layers is so formed as to have
17 a second exposed region in which part of each of said second regions
18 is exposed on a surface of said semiconductor substrate in a manner
19 so as to continuously be in contact with said first exposed region;
20 and

21 wherein each of said silicide layers makes up a low
22 resistance region having a relatively low resistance value, each
23 of said second exposed regions in said second region makes up an
24 intermediate resistance region having an intermediate resistance
25 value, and said first exposed region in said third region makes
26 up a high resistance region having a relatively high resistance
27 value.

1 13. The semiconductor protection element according to Claim 12,
2 wherein a field oxide film is formed on said first surface region

3 or on said first exposed region.

1 14. The semiconductor protection element according to Claim 12,
2 wherein a gate electrode structure is formed on said first surface
3 region or on said first exposed region.

1 15. The semiconductor protection element according to Claim 12,
2 wherein said second exposed region has a surface length being
3 equal to or larger than that of said first exposed region.

1 16. The semiconductor protection element according to Claim 12,
2 wherein a surface length of said second exposed region is equal
3 to or larger than a depth of said second region.

1 17. A method for manufacturing a semiconductor protection
2 element comprising:

3 a first step of implanting an impurity into a semiconductor
4 substrate to form a first region of a first impurity
5 concentration;

6 a second step of forming a pair of second regions having
7 a second impurity concentration being higher than said first
8 impurity concentration on both sides of said first region on a
9 surface of said semiconductor substrate; and

10 a third step of forming silicide layers being in contact
11 with a surface of said second region;

12 wherein, in said third step, each of said silicide layers
13 is formed in a manner that said first region has a first surface
14 region not covered by said silicide layers and said second region
15 has a second surface region not covered by said silicide layers

16 and that said first surface region is sandwiched by two said second
17 surface regions; and

18 wherein each of said silicide layers makes up a low
19 resistance region having a relatively low resistance value, each
20 of said second surface regions makes up an intermediate resistance
21 region having an intermediate resistance value, and said first
22 surface region makes up a high resistance region having a
23 relatively high resistance value.

1 18. A method for manufacturing a semiconductor protection
2 element comprising:

3 a first step of implanting an impurity into a semiconductor
4 substrate to form a first region of a first impurity
5 concentration;

6 a second step of forming a pair of second regions having
7 a second impurity concentration being higher than said first
8 impurity concentration on both sides of a first exposed region
9 being exposed in said first region and on a surface of said
10 semiconductor substrate; and

11 a step of forming each of said silicide layers being in
12 contact with a surface of said second region so that part of each
13 of said second regions is exposed on said surface of said
14 semiconductor substrate succesively so as to be in contact with
15 said first exposed region of said first region;

16 wherein each of said silicide layers makes up a low
17 resistance region having a relatively low resistance value, each
18 of said second exposed regions in said second region makes up an
19 intermediate resistance region having an intermediate resistance
20 value, and said first exposed region in said first region makes

21 up a high resistance region having a relatively high resistance
22 value.

1 19. The method for manufacturing a semiconductor protection
2 element according to Claim 18, wherein each of said second regions
3 and said first region are overlapped each other on a surface of
4 said semiconductor substrate.

1 20. The method for manufacturing a semiconductor protection
2 element according to Claim 19, wherein, said first impurity
3 concentration of said first region, when it is assumed that a well
4 region is formed on said semiconductor substrate, is higher than
5 that of said well region.

1 21. The method for manufacturing a semiconductor protection
2 element according to Claim 18, wherein said second exposed region
3 has a surface length being equal to or larger than that of said
4 first exposed region.

1 22. The method for manufacturing a semiconductor protection
2 element according to Claim 18, wherein a surface length of said
3 second exposed region is equal to or larger than a depth of said
4 second region.

1 23. A method for manufacturing a semiconductor protection
2 element comprising:
3 a step of implanting an impurity into a semiconductor
4 substrate to form a first region of a first impurity
5 concentration;

6 a step of forming a third region having a third impurity
7 concentration being higher than said first impurity concentration
8 in a manner that said third region and said first region are
9 overlapped on a surface of said semiconductor substrate;

10 a step of forming a pair of second regions having a second
11 impurity concentration being higher than that of said third region
12 on both sides of a first exposed region being exposed in said third
13 region and on a surface of said semiconductor substrate;

14 a step of forming each of said silicide layers being in
15 contact with a surface of said second region so that part of each
16 of said second regions is exposed on a surface of said
17 semiconductor substrate successively so as to be in contact with
18 said first exposed region of said first region;

19 wherein each of said silicide layers makes up a low
20 resistance region having a relatively low resistance value, each
21 of said second exposed regions in said second region makes up an
22 intermediate resistance region having an intermediate resistance
23 value, and said first exposed region in said third region makes
24 up a high resistance region having a relatively high resistance
25 value.

1 24. The method for manufacturing a semiconductor protection
2 element according to Claim 23, wherein said second exposed region
3 has a surface length being equal to or larger than that of said
4 first exposed region.

1 25. The method for manufacturing a semiconductor protection
2 element according to Claim 23, wherein a surface length of said
3 second exposed region is equal to or larger than a depth of said

4 second region.

1 26. A semiconductor device comprising:

2 a semiconductor substrate having a first region of a first
3 impurity concentration and a first "second region", second
4 "second region" and third "second region" each having a second
5 impurity concentration being higher than that of said first
6 region;

7 silicide layers each being formed in a manner so as to be
8 in contact with a surface of each of said first "second region",
9 second "second region" and third "second region";

10 one of a source electrode and a drain electrode being formed
11 on one of said silicide layers formed in a manner so as to be in
12 contact with the surface of said first "second region";

13 a gate electrode constructed between said silicide layers
14 formed in a manner so as to be in contact with the surfaces of
15 said first "second region" and second "second region"; and

16 another of said source electrode and said drain electrode
17 being formed on another out of said silicide layers formed in a
18 manner so as to be in contact with the surface of said third "second
19 region";

20 wherein said first region, said second "second region", and
21 said third "second region" have, respectively, a first surface
22 region, second "second surface region", and third "second surface
23 region" all being positioned between said silicide layers formed
24 in a manner so as to be in contact with the surfaces of said second
25 "second region" and third "second region" and all being not
26 covered with said silicide layers;

27 wherein said first surface region is formed in a manner so

28 as to be sandwiched between said second "second surface region"
29 and third "second surface region";

30 wherein each of said silicide layers is constructed in a
31 manner that said second "second surface region" and third "second
32 surface region" are formed so as to be in contact with the surface
33 of said first surface region and so as to expose said second "second
34 surface region" and third "second surface region";

35 wherein each of said silicide layers makes up a low
36 resistance region having a relatively low resistance value, each
37 of said second surface regions makes up an intermediate resistance
38 region having an intermediate resistance value, and said first
39 surface region makes up a high resistance region having a
40 relatively high resistance value.

1 27. The semiconductor device according to Claim 26, wherein a
2 field oxide film is formed on said first surface region or said
3 first exposed region.

1 28. The semiconductor device according to Claim 26, wherein a
2 gate electrode structure is formed on said first surface region
3 or said first exposed region.

1 29. A semiconductor device comprising:

2 a semiconductor substrate having a first region of a first
3 impurity concentration and a first "second region", second
4 "second region" and third "second region" each having a second
5 impurity concentration being higher than that of said first
6 region;

7 silicide layers each being formed in a manner so as to be

8 in contact with a surface of each of said first "second region",
9 second "second region" and third "second region";

10 one of a source electrode and a drain electrode being formed
11 on one of the silicide layers formed in a manner so as to be in
12 contact with the surface of said first "second region";

13 a gate electrode constructed between said silicide layers
14 formed in a manner so as to be in contact with the surfaces of
15 said first "second region" and second "second region"; and

16 another of said source electrode and said drain electrode
17 being formed on another out of said silicide layers formed in a
18 manner so as to be in contact with the surface of said third "second
19 region";

20 wherein said first region has a first exposed region on a
21 surface of said semiconductor substrate between said second
22 "second region" and third "second region";

23 wherein each of said silicide layers is formed so as to have
24 a second exposed region in a manner that said second "second
25 region" and third "second region" are in contact with said second
26 exposed region in a continuous manner;

27 wherein said first exposed region is sandwiched between
28 said second "second region" and third "second region";

29 wherein each of said silicide layers makes up a low
30 resistance region having a relatively low resistance value, each
31 of said second exposed regions in said second "second region" and
32 third "second region" makes up an intermediate resistance region
33 having an intermediate resistance value, and said first exposed
34 region in said first region makes up a high resistance region
35 having a relatively high resistance value.

1 30. The semiconductor device according to Claim 20, wherein
2 said first region is made up of a well region.

1 31. The semiconductor device according to Claim 29, wherein
2 said first region is formed on a surface of said semiconductor
3 substrate and said first region and said second region are
4 overlapped each other on a surface of said semiconductor
5 substrate.

1 32. The semiconductor device according to Claim 31, wherein,
2 said first impurity concentration of said first region, when it
3 is assumed that a well region is formed on said semiconductor
4 substrate, is higher than that of said well region.

1 33. The semiconductor device according to Claim 29, wherein a
2 field oxide film is formed on said first surface region or said
3 first exposed region.

1 34. The semiconductor device according to Claim 29, wherein a
2 gate electrode structure is formed on said first surface region
3 or said first exposed region.

1 35. The semiconductor device according to Claim 29, wherein
2 said second exposed region has a surface length being equal to
3 or larger than that of said first exposed region.

1 36. The semiconductor device according to Claim 29, wherein a
2 surface length of said second exposed region is equal to or larger
3 than a depth of said second region.

1 37. A semiconductor device comprising:

2 a semiconductor substrate having a first region of a first
3 impurity concentration, first "second region", second "second
4 region" and third "second region" each having a second impurity
5 concentration being higher than that of said first region, and
6 a third region having an impurity concentration being higher than
7 said first impurity concentration and being lower than said second
8 impurity concentration;

9 silicide layers each being formed in a manner so as to be
10 in contact with a surface of each of said first "second region",
11 second "second region" and third "second region";

12 one of a source electrode and a drain electrode being formed
13 on one of the silicide layers formed in a manner so as to be in
14 contact with the surface of said first "second region";

15 a gate electrode constructed between said silicide layers
16 formed in a manner so as to be in contact with the surfaces of
17 said first "second region" and second "second region"; and

18 another of said source electrode and said drain electrode
19 being formed on another out of said silicide layers formed in a
20 manner so as to be in contact with the surface of said third "second
21 region";

22 wherein said first region is made up of a well region;

23 wherein said third region is formed on said first region;

24 wherein said third region makes up a first exposed region being
25 exposed on a surface of said semiconductor substrate between said
26 second "second region" and said third "second regions" and, on
27 a surface of said semiconductor substrate, said third region and
28 said second region are overlapped each other;

29 wherein each of said silicide layers is formed so as to have

30 a second exposed region in a manner that said second "second
31 region" and third "second region" are in contact with said first
32 exposed region in a continuous manner;

33 wherein each of said silicide layers makes up a low
34 resistance region having a relatively low resistance value, each
35 of said second exposed regions in said second "second region" and
36 third "second region" makes up an intermediate resistance region
37 having an intermediate resistance value, and said first exposed
38 region in said first region makes up a high resistance region
39 having a relatively high resistance value.

1 38. The semiconductor device according to Claim 37, wherein a
2 field oxide film is formed on said first surface region or said
3 first exposed region.

1 39. The semiconductor device according to Claim 37, wherein a
2 gate electrode structure is formed on said first surface region
3 or said first exposed region.

1 40. The semiconductor device according to Claim 37, wherein
2 said second exposed region has a surface length being equal to
3 or larger than that of said first exposed region.

1 41. The semiconductor device according to Claim 37, wherein a
2 surface length of said second exposed region is equal to or larger
3 than a depth of said second region.

1 42. A method for manufacturing a semiconductor device
2 comprising:

3 a step of implanting an impurity into a semiconductor
4 substrate to form a first region of a first impurity
5 concentration;

6 a step of forming first "second region", second "second
7 region" and third "second region" each having an impurity
8 concentration being higher than said first impurity concentration
9 on said semiconductor substrate and of forming said second "second
10 region" and third "second region" on both sides of said first
11 region on a surface of said semiconductor substrate;

12 a step of forming silicide layers formed in a manner to be
13 in contact with a surface of each of said first "second region",
14 second "second region" and third "second region" in a manner that
15 said first region has a first surface region not covered with said
16 silicide layers and said second "second region" and third "second
17 region" have second surface regions not covered with said silicide
18 layers and said first surface region is sandwiched by two said
19 second surface regions;

20 a step of forming a gate electrode constructed between said
21 silicide layers formed in a manner so as to be in contact with
22 the surfaces of said first "second region" and second "second
23 region";

24 a step of forming one of a source electrode and a drain
25 electrode being formed on the silicide layer formed in a manner
26 so as to be in contact with the surface of said first "second
27 region" and another of said source electrode and said drain
28 electrode being formed on said silicide layer formed in a manner
29 so as to be in contact with the surface of said third "second
30 region";

31 wherein each of said silicide layers makes up a low

32 resistance region having a relatively low resistance value, each
33 of said second surface regions makes up an intermediate resistance
34 region having an intermediate resistance value, and said first
35 surface region makes up a high resistance region having a
36 relatively high resistance value.

1 43. The method for manufacturing a semiconductor device
2 according to Claim 42, further comprising a step of forming a field
3 oxide film formed on said first surface region or said first
4 exposed region.

1 44. The method for manufacturing a semiconductor device
2 according to Claim 42, further comprising a step of forming a gate
3 electrode structure on said first surface region or on said first
4 exposed region.

1 45. A method for manufacturing a semiconductor device
2 comprising:
3 a step of implanting an impurity into a semiconductor
4 substrate to form a first region of a first impurity
5 concentration;
6 a step of forming first "second region", second "second
7 region" and third "second region" each having an impurity
8 concentration being higher than said first impurity concentration
9 on said semiconductor substrate and said second "second region"
10 and third "second region" are formed on a surface of said
11 semiconductor substrate on both sides of said first exposed region
12 so that said first region has a first exposed region being exposed
13 on a surface of said semiconductor substrate;

14 a step of forming each of said silicide layers being in
15 contact with a surface of each of said first "second region",
16 second "second region" and third "second region" so that said
17 second "second region" and third "second region" so as to have
18 a second exposed region being successively in contact with said
19 first exposed region of said first region;

20 a step of forming a gate electrode constructed between said
21 silicide layers formed in a manner so as to be in contact with
22 surfaces of said first "second region" and second "second region";

23 a step of forming one of a source electrode and a drain
24 electrode being formed on the silicide layer formed in a manner
25 so as to be in contact with a surface of said first "second region"
26 and another of said source electrode and said drain electrode
27 being formed on said silicide layer formed in a manner so as to
28 be in contact with the surface of said third "second region";

29 wherein each of said silicide layers makes up a low
30 resistance region having a relatively low resistance value, each
31 of said second exposed regions in said second region makes up an
32 intermediate resistance region having an intermediate resistance
33 value, and said first exposed region in said first region makes
34 up a high resistance region having a relatively high resistance
35 value.

1 46. The method for manufacturing a semiconductor device
2 according to Claim 45, wherein said second region are formed on
3 a surface of said semiconductor substrate in a manner that said
4 second region and said first region are overlapped.

1 47. The method for manufacturing a semiconductor device

2 according to Claim 46, wherein, said first impurity concentration
3 of said first region, when it is assumed that a well region is
4 formed on said semiconductor substrate, is higher than that of
5 said well region.

1 48. The method for manufacturing a semiconductor device
2 according to Claim 45, wherein a surface length of said second
3 exposed region is equal to or larger than a depth of said second
4 region.

1 49. The method for manufacturing a semiconductor device
2 according to Claim 45, wherein a surface length of said second
3 exposed region is equal to or larger than a depth of said second
4 region.

1 50. The method for manufacturing a semiconductor device
2 according to Claim 45, further comprising a step of forming a field
3 oxide film formed on said first surface region or said first
4 exposed region.

1 51. The method for manufacturing a semiconductor device
2 according to Claim 45, further comprising a step of forming a gate
3 electrode structure on said first surface region or on said first
4 exposed region.

1 52. A method for manufacturing a semiconductor device
2 comprising:

3 a step of implanting an impurity into a semiconductor
4 substrate to form a first region of a first impurity

5 concentration;

6 a step of forming a third region having a thirs impurity
7 concentration being higher than said first impurity concentration
8 in a manner that said third region and said first region are
9 overlapped on a surface of said semiconductor substrate;

10 a step of forming first "second region", second "second
11 region" and third "second region" each having a second impurity
12 concentration being higher than said third impurity concentration
13 in said third region on said semiconductor substrate and said
14 second "second region" and third "second region" are formed on
15 a surface of said semiconductor substrate on both sides of said
16 first exposed region so that said third region has a first exposed
17 region being exposed on a surface of said semiconductor substrate;

18 a step of forming each of said silicide layers being in
19 contact with a surface of each of said first "second region",
20 second "second region" and third "second region" so that said
21 second "second region" and third "second region" are exposed
22 successively so as to be in contact with said first exposed region
23 of said first region;

24 a step of forming a gate electrode constructed between said
25 silicide layers formed in a manner so as to be in contact with
26 the surfaces of said first "second region" and second "second
27 region";

28 a step of forming one of a source electrode and a drain
29 electrode being formed on one of the silicide layers formed in
30 a manner so as to be in contact with the surface of said first
31 "second region" and another of said source electrode and said
32 drain electrode being formed on another out of said silicide
33 layers formed in a manner so as to be in contact with the surface

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34 of said third "second region";

35 wherein each of said silicide layers makes up a low
36 resistance region having a relatively low resistance value, each
37 of said second exposed regions in said second region makes up an
38 intermediate resistance region having an intermediate resistance
39 value, and said first exposed region in said third region makes
40 up a high resistance region having a relatively high resistance
41 value.

1 53. The method for manufacturing a semiconductor device
2 according to Claim 52, wherein a surface length of said second
3 exposed region is equal to or larger than a depth of said second
4 region.

1 54. The method for manufacturing a semiconductor device
2 according to Claim 52, wherein a surface length of said second
3 exposed region is equal to or larger than a depth of said second
4 region.

1 55. The method for manufacturing a semiconductor device
2 according to Claim 52, further comprising a step of forming a field
3 oxide film formed on said first surface region or said first
4 exposed region.

1 56. The method for manufacturing a semiconductor device
2 according to Claim 52, further comprising a step of forming a gate
3 electrode structure on said first surface region or on said first
4 exposed region.